Appl. No. 10/690,859
Examiner: LE, THAO P, Art Unit 2818
In response to the Office Action dated February 23, 2005

Date: May 23, 2005
Attorney Docket No. 10113101

**REMARKS**

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority and receipt of the certified copy of the priority document. Responsive to the Office Action mailed on February 23, 2005 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-4, 6-9, 10-12 and 15-17 stand rejected under 35 U.S.C. 102(a) as being anticipated by Hong et al (US 6,566,229, hereinafter "Hong-1"). Claims 5 and 14 stand rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1. Claim 13 stands rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Hong et al. (US 6,593,207, hereinafter "Hong-2"). Claims 18-26, 27-29, 31-35 stand rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Lin et al. (US 6,713,365, hereinafter "Lin et al"). Claim 30 stands rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Lin et al and in further view of Hong-2. Claims 36-41 stand rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Hong-2. Claims 42-48 stand rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Hong-2, and further in view of Lin.

After this amendment, claims 1-2, 5-19, and 22-48 are pending. Claims 1, 6, 7, 10, 18, 24, 27, 36 and 42 are amended. Support for the amendments can be found on page 7, lines 3-7 of the specification and in the original claims. Claims 3, 4, 20 and 21 are cancelled.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

The rejections of claims 1-48 are insufficient, insofar as they are based on a mischaracterization of the prior art and therefore do not comply with the requirements of MPEP 707.07 *et seq.*, which requires that all rejections be stated with completeness and clarity.

In the rejection of original claims 3-4, 10, 20-21, 27, 36 and 42 of the present application, the Examiner asserts that Hong-1 teach forming LPCVD oxide layer 21 to cover the substrate and the trench. The Examiner refers to columns 3 and 4 of Hong-1 is support of this characterization of the prior art.

However, as described in further detail in the following sections, Hong-1 teach forming a polysilazane solution is coated on a substrate 10 by a spin on glass (SOG) manner to form an SOG layer 21 filling a trench 19. See column 3, line 58-66 of Hong-1. Thus, it is clear that layer 21 is not an oxide layer formed by LPCVD, as characterized by the Examiner in the rejections of the claims, but rather an SOG layer formed from a polysilazane solution. All of the rejections of the claims as currently pending are based upon this mischaracterization of the prior art.

Applicant therefore respectfully requests the withdrawal of the rejection of claims 10, 27, 36 and 42. Furthermore, as claim 1 has been amended to include the limitations of original claims 3 and 4, and claim 18 has been amended to include the limitations of original claims 20 and21, Applicant respectfully request withdrawal of the rejections of claims 1 and 18.

Should an ensuing office action be mailed which provides new grounds for the rejection of claims 1-48, such action should be made non-final.

Rejections Under 35 U.S.C. 102(a)

Claims 1-4, 6-9, 10-12 and 15-17 stand rejected under 35 U.S.C. 102(a) as being anticipated by Hong-1. The rejections are respectfully traversed for the reasons as follow.

Hong-1 teach a method of forming an insulating layer in a trench isolation type semiconductor device. In Hong-1, a polysilazane solution is coated on a substrate 10 by a spin on glass (SOG) manner to form an SOG layer 21 filling a trench 19 formed in the substrate. See column 3, line 57 to column 4, line 20 and Fig. 2 of Hong-1. The SOG layer 21 is cured and etched to form SOG layer 211 recessed below the top level of the substrate. See column 4, lines 57-64 and Fig. 3 of Hong-1. Subsequently, a silicon oxide layer 31 is deposited on SOG layer 211. See column 5, lines 19-27 and Fig. 4 of Hong-1.

Further, Hong-1 teach in column 2, lines 7-17:

> "In an effort to overcome the foregoing disadvantages, it has been proposed to form a layer of LPCVD TEOS in a trench that is partially filled with HSQ, see "Shallow Trench Isolation Fill for 1 Gbit DRAM and Beyond Using a Hydrogen Silsesquioxane Glass/LPCVD TEOS Hybrid Approach," contributed to the DUMIC Conference by IBM, 1998. Unfortunately, such an approach requires a separate processing because the conformality of the coating is reduced. If filling a trench with HSQ is beyond a reasonable degree, defects are possibly formed in subsequent process steps."

Hong-1 do not teach or suggest a method for forming a trench isolation, comprising the steps of, *inter alia*, forming a LPCVD oxide layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the LPCVD oxide layer, anisotropically etching the LPCVD oxide layer to below the level of the semiconductor substrate, and forming an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench, as recited in claim 1.

MPEP 2131 prescribes that to anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In Hong-1, a polysilazane solution is coated on a semiconductor substrate in a spin on glass (SOG) manner to form an SOG layer filling a trench. A CVD type silicon oxide layer is stacked on the SOG layer to fill a remaining portion of the trench. Thus, in Hong-1, a trench is first filled with a SOG layer and then a LPCVD layer is formed on the etched SOG layer.

Thus, Hong-1 fail to teach a method for forming a trench isolation including the step of forming a LPCVD oxide layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the LPCVD oxide layer, as recited in claim 1. Hong-1 further fail to teach a method for forming a trench isolation further including the step of anisotropically etching the LPCVD oxide layer to below the level of the semiconductor substrate, as recited in claim 1. Finally, Hong-1 fail to teach or suggest a method for forming a trench isolation further including the step of forming an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench, as recited in the claim 1.

For at least this reason, it is Applicant's belief that claim 1 is allowable over the cited reference. Insofar as claim 2 and 5-9 depend from claim 1, it is Applicant's belief that these claims are also in condition for allowance.

Hong-1 do not teach or suggest a method for forming a trench isolation comprising, *inter alia*, the steps of conformably forming an LPCVD oxide layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the LPCVD oxide layer, anisotropically etching the LPCVD oxide layer to lower its surface below a top surface of the semiconductor substrate by at least 300Å, and forming an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench, wherein the trench is filled with the insulating layer, as recited in claim 10.

For the same reasons discussed in connection with claim 1, it is Applicant's belief that the cited references fail to teach or suggest all the limitations recited in claim 10. It is therefore Applicant's belief that claim 10 is allowable over the cited references. Insofar as claims 11-17 depend from claim 10, it is Applicant's belief that these claims are also in condition for allowance.

Rejections Under 35 U.S.C. 103(a)

Claims 5 and 14 stand rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1. Claim 13 stands rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Hong-2. Claims 18-26, 27-29, 31-35 stand rejected under 35 U.S.C. 103(a) as being anticipated by

Hong-1 in view of Lin et al. Claim 30 stands rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Lin et al and in further view of Hong-2. Claims 36-41 stand rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Hong-2. Claims 42-48 stand rejected under 35 U.S.C. 103(a) as being anticipated by Hong-1 in view of Hong-2, and further in view of Lin.

For the reasons discussed above, claims 5, 13, and 14 are believed to be allowable by virtue of their dependency from claims 1 and 10. For this reason, the Examiner's arguments in connection with these claims are considered moot and will not be addressed here.

None of Hong-1 or Lin et al, when taken alone or in combination, teach or suggest a method for forming a trench isolation comprising the steps of, *inter alia*, forming a LPCVD oxide layer to cover the semiconductor substrate and the trench, anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the trench, and forming an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench, as recited in claim 18.

MPEP 2142 reads in part:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of

that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

In Hong-1, a polysilazane solution is coated on a semiconductor substrate in a spin on glass (SOG) manner to form an SOG layer filling a trench. A CVD type silicon oxide layer is stacked on the SOG layer to fill a remaining portion of the trench. Thus, in Hong-1, a trench is first filled with a SOG layer and then a LPCVD layer is formed on the etched SOG layer.

Neither Hong-2 nor Lin et al teach or suggest forming a LPCVD oxide layer to cover the semiconductor substrate and the trench, anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the trench, and forming an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench, as recited in claim 18.

For at least these reasons, it is Applicant's belief that claim 18 is allowable over the cited references. Insofar as claims 19 and 22-26 depend from claim 18, it is Applicant's belief that these claims are also in condition for allowance.

None of Hong-1 or Lin et al, when taken alone or in combination, teach or suggest a method for forming a trench isolation comprising the steps of, *inter alia*, conformably forming an LPCVD oxide layer to cover the semiconductor substrate and the trench, anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the trench, and forming an insulating layer to cover the semiconductor substrate and LPCVD oxide layer in the trench, as recited in claim 27.

For the same reasons discussed in connection with claim 18, it is Applicant's belief that the cited references fail to teach or suggest all the limitations recited in claim 27. It is therefore Applicant's belief that claim 27 is allowable over the cited references. Insofar as claims 28-35 depend from claim 27, it is Applicant's belief that these claims are also in condition for allowance.

None of Hong-1 or Hong-2, when taken alone or in combination, teach or suggest a method for forming a trench isolation comprising the steps of, *inter alia*, conformably forming an LPCVD

oxide layer to cover the semiconductor substrate, the first trench, and the second trench, wherein the first trench is filled with the LPCVD oxide layer, anisotropical etching the LPCVD oxide layer to lower its surface below a top surface of the semiconductor substrate by at least 300Å, and forming an insulating layer to cover the semiconductor substrate, the LPCVD oxide layer in the first trench and the LPCVD oxide layer in the second trench, as recited in claim 36.

For the same reasons discussed in connection with claim 18, it is Applicant's belief that the cited references fail to teach or suggest all the limitations recited in claim 36. It is therefore Applicant's belief that claim 36 is allowable over the cited references. Insofar as claims 37-41 depend from claim 36, it is Applicant's belief that these claims are also in condition for allowance.

None of Hong-1, Hong-2 or Lin et al, when taken alone or in combination, teach or suggest a method for forming a trench isolation comprising the steps of, *inter alia*, conformably forming an LPCVD oxide layer to cover the semiconductor substrate, anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the first trench, and forming an insulating layer to cover the semiconductor substrate, the LPCVD oxide layer in the first trench and the LPCVD oxide layer in the second trench, as recited in claim 42.

For the same reasons discussed in connection with claim 18, it is Applicant's belief that the cited references fail to teach or suggest all the limitations recited in claim 42. It is therefore Applicant's belief that claim 42 is allowable over the cited references. Insofar as claims 43-48 depend from claim 42, it is Applicant's belief that these claims are also in condition for allowance.

Foreign Priority Claim

Applicant notes that this application claims priority from **Taiwan** application serial no. 92120043.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

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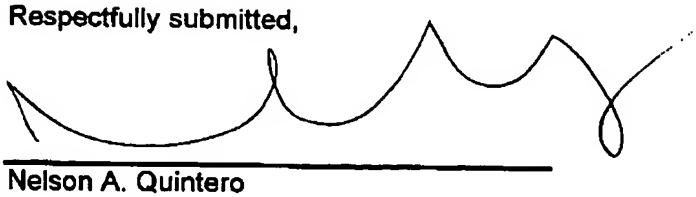
Respectfully submitted,



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